FORCE COMPUTERS
A SOLECTRON COMPANY

SPARC/CPU-8VT

Installation Guide

P / N 204721 Revision AC
November 2001

Copyright

The information in this publication is subject to change without notice. Force Computers, GmbH reserves the right to make changes without notice to this, or any of its products, to improve reliability, performance, or design.

Force Computers, GmbH shall not be liable for technical or editorial errors or omissions contained herein, nor for indirect, special, incidental, or consequential damages resulting from the furnishing, performance, or use of this material. This information is provided “as is” and Force Computers, GmbH expressly disclaims any and all warranties, express, implied, statutory, or otherwise, including without limitation, any express, statutory, or implied warranty of merchantability, fitness for a particular purpose, or non-infringement.

This publication contains information protected by copyright. This publication shall not be reproduced, transmitted, or stored in a retrieval system, nor its contents used for any purpose, without the prior written consent of Force Computers, GmbH.

Force Computers, GmbH assumes no responsibility for the use of any circuitry other than circuitry that is part of a product of Force Computers, GmbH. Force Computers, GmbH does not convey to the purchaser of the product described herein any license under the patent rights of Force Computers, GmbH nor the rights of others.

Copyright© 2001 by Force Computers, GmbH. All rights reserved.

The Force logo is a trademark of Force Computers, GmbH.

IEEE is a registered trademark of the Institute for Electrical and Electronics Engineers, Inc.
PICMG, CompactPCI, and the CompactPCI logo are registered trademarks and the PICMG logo is a trademark of the PCI Industrial Computer Manufacturer’s Group.
MS-DOS, Windows95, Windows98, Windows2000 and Windows NT are registered trademarks and the logos are a trademark of the Microsoft Corporation.
Intel and Pentium are registered trademarks and the Intel logo is a trademark of the Intel Corporation.

Other product names mentioned herein may be trademarks and / or registered trademarks of their respective companies.

World Wide Web: www.forcecomputers.com
24-hour access to on-line manuals, driver updates, and application notes is provided via SMART, our SolutionsPLUS customer support program that provides current technical and services information.

Headquarters

The Americas

Force Computers Inc.
5799 Fontanoso Way
San Jose, CA 95138-1015
U.S.A.

Tel.: +1 (408) 369-6000
Fax: +1 (408) 371-3382
Email: support@fci.com

Europe

Force Computers GmbH
Prof.-Messerschmitt-Str. 1
D-85579 Neubiberg/München
Germany

Tel.: +49 (89) 608 14-0
Fax: +49 (89) 609 77 93
Email: support@force.de

Asia

Force Computers Japan KK
Shiba Daimon MF Building 4F
2-1-16 Shiba Daimon
Minato-ku, Tokyo 105-0012 Japan

Tel.: +81 (03) 3437 3948
Fax: +81 (03) 3437 3968
Email: smiyagawa@fci.com

204721 420 000 AC

Table of Contents

Using This Manual . . . . . **v**

Safety Notes . . . . . **ix**

Sicherheitshinweise . . . . . **xiii**

1 Installation **1**

1.1 Installation Prerequisites and Requirements **1**

1.1.1 Requirements 1

1.1.2 Terminal Connection 1

1.1.3 Location Overview 1

1.2 Switch Settings **3**

1.2.1 Memory Module MEM-5 5

1.3 Power Up **6**

1.3.1 VME Slot-1 Device 6

1.3.2 VMEbus SYSRESET 6

1.3.3 Serial Ports 7

1.3.4 RESET and ABORT Key Enable 7

1.3.5 Boot Flash Memory Write Protection 7

1.3.6 User Flash Memory Write Protection 7

1.3.7 Reserved Switches 7

1.3.8 Floppy Interface or SCSI #2 Availability on P2 8

1.3.9 Network Interface Selection (NIS) for Ethernet 9

1.3.10 Parallel Port 9

1.4 SCSI Configuration **9**

1.4.1 SCSI #1 Termination 9

1.4.2 SCSI #2 Termination 11

1.5 Connectors 13

1.5.1 Twisted Pair Ethernet Connector Pinout 13

1.5.2 Serial Port A and B Connector Pinout 14

1.5.3 Keyboard/Mouse Connector Pinout 14

1.5.4 VME P2 Connector Pinout 15

1.6 IOBP-10 16

1.6.1 Jumper Setting for IOBP-10 16

1.6.2 IOBP-10 Connector Pinouts 17

1.7 IOBP-DS 19

1.7.1 Jumper Setting for IOBP-DS 19

1.7.2 IOBP-DS Connector Pinouts 20

1.8 Ethernet Address and Host ID 22

1.9 OpenBoot Firmware 23

1.9.1 Boot the System 23

1.9.2 NVRAM Boot Parameters 25

1.9.3 Diagnostics 26

1.9.4 Display System Information 28

1.9.5 Reset the System 29

1.9.6 OpenBoot Help 30

Product Error Report

List of Tables and Figures

	Page	Tab./Fig.
History of Manual Publication	vi	Tab. a
Fonts, Notations and Conventions	vi	Tab. b
Location Diagram of the SPARC/CPU-8VT (Schematic)	2	Fig. 1
Default Switch Settings	3	Tab. 1
Floppy or SCSI #2 Availability on P2	8	Fig. 2
SPARC/CPU-8VT Connectors	13	Tab. 2
Twisted Pair Ethernet Connector Pinout	13	Fig. 3
Serial Port A and B Connector Pinout	14	Fig. 4
Keyboard/Mouse Connector Pinout	14	Fig. 5
VME P2 Connector Pinout	15	Fig. 6
The IOBP-10 Back Panel	16	Fig. 7
IOBP-10 P1 Pinout	17	Fig. 8
IOBP-10 P2 Pinout (SCSI #1)	17	Fig. 9
IOBP-10 P3 Pinout (Floppy)	18	Fig. 10
IOBP-10 P5 Pinout (Serial A and B)	18	Fig. 11
IOBP-10 P6 Pinout (Ethernet #1 – AUI)	18	Fig. 12
The IOBP-DS Back Panel	19	Fig. 13
IOBP-DS P2 Pinout	20	Fig. 14
IOBP-DS J1 Pinout (SCSI #1)	20	Fig. 15
IOBP-DS J2 Pinout (SCSI #2)	21	Fig. 16
IOBP-DS J3 Pinout (Ethernet #1 – AUI)	21	Fig. 17
IOBP-DS J4 Pinout (Serial A and B)	21	Fig. 18
IOBP-DS J5 Pinout (Keyboard/mouse)	21	Fig. 19
The 48-bit (6-byte) Ethernet Address	22	Fig. 20
The 32-bit (4-byte) Host ID	22	Fig. 21
Device Alias Definitions	24	Tab. 3
Setting Configuration Parameters	25	Tab. 4
Diagnostic Routines	26	Tab. 5
Commands to display System Information	29	Tab. 6

Page **Tab./Fig.**

Using This Manual

This section does not provide information on the product, but on standard features of the manual itself:

- its structure,
- special layout conventions,
- and related documents.

Audience of the Manual and Overview of the Manual

This *Installation Guide* is intended for hard- and software developers as well as support and service engineers installing the SPARC/CPU-8VT. It is packaged and shipped together with the product.

IMPORTANT

Please take a moment to examine the Table of Contents to see how this documentation is structured. This will be of value to you when looking for information in the future.

This *Installation Guide* includes the installation instructions for powering up the board, in detail:

- the default configuration of the board, for example, the default switch setting
- initialization prerequisites and procedures
- connector pinouts

SPARC/CPU-8VT Technical Reference Manual

The installation instructions are also published in the product's *Technical Reference Manual* – a separate manual delivered as separate price list item. The *Technical Reference Manual* includes:

- an overview of the product, its specification and ordering information
- a detailed hardware description
- the circuit schematics of the SPARC/CPU-8VT
- a detailed software description

Publication History of the Manual

Table a **History of Manual Publication**

Edition/ Revision	Date	Description
1.0	March 1997	First Print
2.0	December 1998	P2 factory option changed from 5-row to 3-row and 5-row became the standard.
3.0/AA	December 2000	Safety Notes added; editorial changes
4.0/AB	August 2001	Corrected Safety Notes; Added chapter Sicherheitshinweise
AC	November 2001	Editorial changes

Fonts, Notations and Conventions

Table b **Fonts, Notations and Conventions**

Notation	Description
	All numbers are decimal numbers except when used with the following notations:
0000.0000_{16}	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets. Note the dot marking the 4th (to its right) and 5th (to its left) digit.
0000_{8}	Same for octal numbers (digits are 0 through 7)
0000_{2}	Same for binary numbers (digits are 0 and 1)
`Program`	Typical character format used for names, values, and the like. It is used to indicate when to type literally the same word. Also used for on-screen output.
Variable	Typical character format for words that represent a part of a command, a programming statement, or the like, and that will be replaced by an applicable value when actually applied.

Icons for Ease of Use: Safety Notes and Tips & Tricks

There are 3 levels of safety notes used in this manual which are described below in short by displaying a typical layout example.

Be sure, to always read and follow the safety notes of a section first – before acting as documented in the other parts of the section.

CAUTION

Dangerous situation: injuries to people and severe damage to objects possible.

NOTICE

Possibly dangerous situation: no injuries to people but damage to objects possible.

IMPORTANT

No danger encountered. Only application hints and time-saving tips & tricks or information on typical errors when using the information mentioned below this safety hint.

Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the SPARC/CPU-8VT. For your protection, follow all warnings and instructions found in the following text.
This Installation Guide provides the necessary information to install and handle the SPARC/CPU-8VT. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Force Computers representative.

The SPARC/CPU-8VT has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, uninstall or maintain the SPARC/CPU-8VT. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The board has been tested in a Standard Force Computers system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules respectively EN 55022 Class A.

These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

The board generates, uses and can radiate radio frequency energy and, if not installed properly and used in accordance with this Installation Guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

If boards are integrated into open systems, always cover empty slots.

To ensure proper EMC shielding, always operate the SPARC/CPU-8VT with the blind panels or with PMC modules installed.

Installation

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their life. Therefore:

- **Before touching integrated circuits, make sure that you are working in an ESD-safe environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or uninstalling an additional device or module, read the respective documentation.**
- **Make sure that the board is connected to the VMEbus backplane via all assembled connectors and that power is available on all power pins.**

Operation

While operating the board ensure that the environmental and power requirements are met.

When operating the board in areas of strong electromagnetic radiation ensure that the board is bolted on the VME rack and shielded by enclosure.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Expansion

Check the total power consumption of all components installed (see the technical specification of the respective components).

Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).

Only replace components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMI and the possibly changed functionality of the product.

RJ-45 Connector

An RJ-45 connector is used for both telephone and twisted pair Ethernet (TPE) connectors. Mismatching the two connectors may destroy your telephone as well as your SPARC/CPU-8VT. Therefore:

- **TPE connectors near your working area have to be clearly marked as network connectors.**
- **TPE bushing of the system has to be connected only to safety extra low voltages (SELV) circuits.**
- **The length of the electric cable connected to a TPE bushing must not exceed 100 meter.**

Battery

If a Lithium battery on the board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Always use the same type of Lithium battery as is already installed.**

Environment

Always dispose of used batteries and/or old boards according to your country's legislation.

Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, welche bei der Installation, dem Betrieb und der Wartung des SPARC/CPU-8VT zu beachten sind. Beachten Sie zu Ihrem Schutz alle folgenden Warnhinweise und Anleitungen.

Dieses Installationshandbuch enthält alle notwendigen Informationen zur Installation und zum Betrieb des SPARC/CPU-8VT. Da es sich um ein komplexes Produkt mit einer aufwendigen Bedienung handelt, kann keine Garantie dafür übernommen werden, dass die enthaltenen Informationen vollständig sind. Für weitere Informationen wenden Sie sich bitte an Ihren Vertreter der Firma Force Computers.

Das SPARC/CPU-8VT erfüllt die gültigen industriellen Sicherheitsanforderungen. Dieses Produkt darf ausschließlich für Anwendungen innerhalb der Telekommunikationsindustrie und der industriellen Steuerung verwendet werden.

Lediglich von Force Computers eingewiesene oder im Bereich Elektrotechnik oder Elektronik qualifizierte Personen sind zur Installation, zum Betrieb und zur Wartung dieses Produktes befugt. Die in dieser Dokumentation enthaltenen Informationen sollen lediglich als Hilfestellung für entsprechend qualifiziertes Fachpersonal dienen. Keinesfalls können sie dieses ersetzen.

EMV

Das Board wurde in einem Force Computers Standardsystem getestet und entspricht den Grenzen eines Klasse-A-Produktes gemäß Abschnitt 15 der FCC-Richtlinien, insbesondere EN 55022 Klasse A.

Diese Grenzen sind dafür vorgesehen, einen vernünftigen Schutz gegen störende Einflüsse bei einem Betrieb in einer kommerziellen Umgebung zu gewährleisten.

Das Board erzeugt elektromagnetische Strahlung. Wird das System un-sachgemäß installiert oder in anderer Weise als in diesem Installationshandbuch beschrieben betrieben, kann es in der Umgebung von Rundfunksendern und in Wohngegenden zu Störungen kommen. In diesem Fall ist der Benutzer verpflichtet, entstehende Störungen auf seine Kosten beheben zu lassen und die Kosten von Messungen selbst zu tragen.

Werden Boards in offene Systeme eingebaut, müssen freie Steckplätze mit einer Blende abgeschirmt werden.

Um eine ausreichende Abschirmung zu gewährleisten, darf das Board nur mit einer Blindblende oder mit einer installierten PCMCIA-Karte betrieben werden.

Installation

Elektrostatische Entladung und unsachgemäße Installation und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Deswegen sind folgende Punkte vor der Installation zu überprüfen:

- **Bevor Sie integrierte Schaltkreise berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Drücken Sie beim Einbau oder Ausbau des Boards nicht auf das Front Panel, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor dem Einbau oder Ausbau von zusätzlichen Geräten oder Modulen das jeweilige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die VMEbus Backplane angeschlossen ist und Strom an allen Power Pins anliegt.**

Betrieb

Während des Betriebs müssen die Umgebungs- und die Stromsversorgungsbedingungen gewährleistet sein.

Wenn das Board in Gebieten mit starker elektromagnetischer Strahlung betrieben wird, stellen Sie sicher, dass das Board auf dem VME Rack verschraubt ist und mit einem Gehäuse geschützt ist.

Es ist sicherzustellen, dass Anschlüsse und Kabel des Boards während des Betriebs nicht versehentlich berührt werden können.

Erweiterung

Beachten Sie den Gesamtstromverbrauch aller installierter Komponenten (siehe technische Daten der entsprechenden Komponente).

Vergewissern Sie sich, daß jeder individuelle Ausgangsstrom jedes Stromverbrauchers innerhalb der zulässigen Grenzwerte liegt (siehe technische Daten des entsprechenden Verbrauchers).

Benutzen Sie bei der Erweiterung ausschließlich von Force Computers empfohlene Komponenten und Systemteile. Ansonsten sind Sie für die Auswirkungen auf EMV und die möglicherweise geänderte Funktionalität des Produktes verantwortlich.

RJ-45 Stecker

RJ-45 Stecker werden sowohl für Telefonanschlüsse als auch für Twisted-pair-Ethernet (TPE) verwendet. Die Verwechslung solcher Anschlüsse kann sowohl das Telefonsystem als auch das Board zerstören. Daher:

- **TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes müssen deutlich als Netzwerkanschlüsse gekennzeichnet sein.**
- **An TPE-Buchsen dürfen nur SELV-Kreise angeschlossen werden (Sicherheitskleinspannungsstromkreise).**
- **Die Länge der an einer TPE-Buchse angeschlossenen Leitung darf nicht mehr als 100 Meter betragen.**

Batterie

Muss eine Lithium Batterie auf dem Board ausgetauscht werden, müssen die folgenden Sicherheitshinweise beachtet werden:

- **Fehlerhafter Austausch von Lithium Batterien kann zu lebensgefährlichen Explosionen führen.**
- **Es darf nur der Batterietyp verwendet werden, der auch bereits eingesetzt ist.**

Umweltschutz

Alte Batterien und/oder Boards oder Systeme müssen stets gemäß der in Ihrem Land gültigen Gesetzgebung entsorgt werden.

1 Installation

1.1 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements
- and check the consistency of the current switch setting (see section 1.2 “Switch Settings” on page 3).

1.1.1 Requirements

The installation requires only

- a power supply
- and a VMEbus backplane with P1 and P2 connectors.

Power Supply

The power supply must meet the following specifications:

- required for the processor board: +5V
  - 5.2 A typical
- required for the RS-232 serial interface:
  - +12 V (0.1 A typical)
  - –12 V (0.1 A typical)

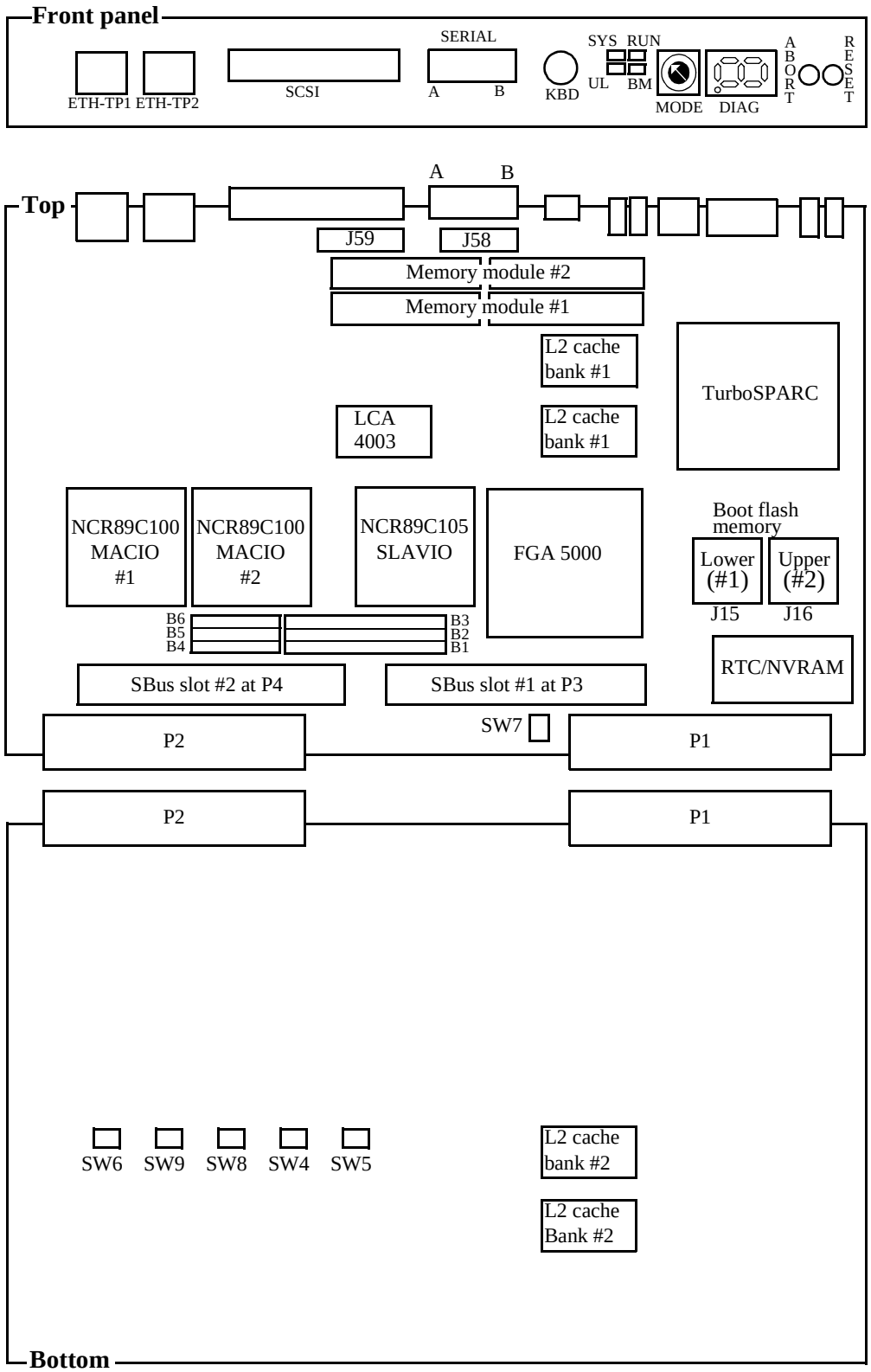
1.1.2 Terminal Connection

For the initial power-up, a terminal can be connected to the 26-pin MicroD-Sub connector of the serial port, which is located at the front panel (see section 1.3.3 “Serial Ports” on page 7 and section 1.5.2 “Serial Port A and B Connector Pinout” on page 14).

1.1.3 Location Overview

The figure 1 “Location Diagram of the SPARC/CPU-8VT (Schematic)” on page 2 highlights the position of the important SPARC/CPU-8VT components. Depending on the board type it might be that your board does not include all components named in the location diagram.

Figure 1 Location Diagram of the SPARC/CPU-8VT (Schematic)



1.2 Switch Settings

The following table lists the functions and the default settings of all switches shown in figure 1 “Location Diagram of the SPARC/CPU-8VT (Schematic)” on page 2.

IMPORTANT

- Before powering up the board check the current switch settings for consistency.
- Do not switch during operation.

Table 1 Default Switch Settings

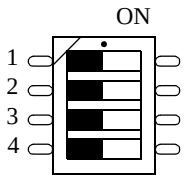
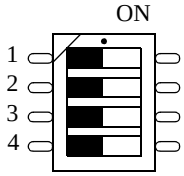
Name and default setting		Function
Serial A config. 	SW4-1 OFF	OFF = TRXC on front-panel connector for RS-232 ON = reserved for RS-485
	SW4-2 OFF	OFF = CTS (CTS+/-) on front-panel connector for RS-232 (RS-422) ON = RTXC +/- on front-panel connector for RS-422
	SW4-3 OFF	OFF = RTS (RTS+/-) on front-panel connector for RS-232 (RS-422) ON = TRXC +/- on front-panel connector for RS-422
	SW4-4 OFF	reserved: must be OFF.
Serial B config. 	SW5-1 OFF	OFF = TRXC on front-panel connector for RS-232 ON = reserved for RS-485
	SW5-2 OFF	OFF = CTS (CTS+/-) on front-panel connector for RS-232 (RS-422) ON = RTXC +/- on front-panel connector for RS-422
	SW5-3 OFF	OFF = RTS (RTS+/-) on front-panel connector for RS-232 (RS-422) ON = TRXC +/- on front-panel connector for RS-422
	SW5-4 OFF	reserved; must be OFF.

Table 1 Default Switch Settings (cont.)

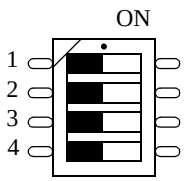
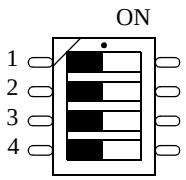
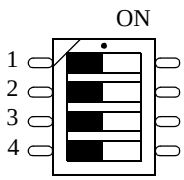
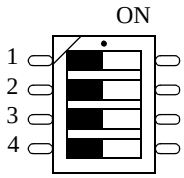
Name and default setting		Function
	SW6-1 OFF	SCSI Termination for SCSI #1 on front panel OFF = SCSI-Term front panel automatic ON = SCSI-Term front panel disabled
	SW6-2 OFF	SCSI Termination for SCSI #1 on P2 OFF = disabled ON = enabled
	SW6-3 OFF	SCSI Termination for SCSI #2 on P2 OFF = enabled ON = disabled
	SW6-4 OFF	Reset key on front-panel control OFF = RESET key enabled ON = RESET key disabled
	SW7-1 OFF	VMEbus SYSRESET on power-up OFF = enabled ON = disabled
	SW7-2 OFF	External VMEbus SYSRESET OFF = VMEbus SYSRESET generates on-board RESET ON = VMEbus SYSRESET does not generate on-board RESET
	SW7-3 OFF	VMEbus SYSRESET generation OFF = SYSRESET is driven to VMEbus ON = SYSRESET is not driven to VMEbus
	SW7-4 OFF	Abort key control OFF = ABORT key enabled ON = ABORT key disabled

Table 1 Default Switch Settings (cont.)

Name and default setting		Function
	SW8-1 OFF	Automatic VMEbus slot-1 detection OFF = Automatic detection of VME Slot 1 function ON = Automatic detection of VME slot 1 function disabled. Use SW8-2 instead.
	SW8-2 OFF	Manual VMEbus slot-1 selection OFF = VME slot 1 function enabled ON = VME slot 1 function disabled SW8-2 is active only when SW8-1 = ON!
	SW8-3 OFF	Test switch, must be OFF
	SW8-4 OFF	Voltage sensor sensibility select OFF = Power sense 4.75V ON = Power sense 4.5V
	SW9-1 OFF	Boot flash EPROM write protection OFF = Write boot flash disabled ON = Write boot flash enabled
	SW9-2 OFF	User flash EPROM write protection OFF = Write user flash disabled ON = Write user flash enabled
	SW9-3 OFF	Local LCA configuration mode OFF = LCA configuration mode serial PROM ON = LCA configuration mode download
	SW9-4 OFF	Test switch, must be OFF

1.2.1 Memory Module MEM-5

Per default, memory module #1 is already installed on the delivered CPU board. The memory module #1 is required for powering up because it holds configuration information for booting the board. Memory module #2 is optional for increasing memory capacity. For instructions on installing the MEM-5, see the *How to Install MEM-5 Installation Guide.*
For the location of the memory module connectors on the board, see figure 1 “Location Diagram of the SPARC/CPU-8VT (Schematic)” on page 2.

1.3 Power Up

The initial power up can easily be done by connecting a terminal to TTYA (serial port A). The advantage of using a terminal is that no frame buffer, monitor, or keyboard is used for initial power up, which facilitates a simple start-up.

IMPORTANT

For the initial power up, do not connect a keyboard to the board when using TTYA (serial port A). For more detailed information on booting the system, see section 1.9.1 “Boot the System” on page 23.

1.3.1 VME Slot-1 Device

Automatic VME Slot-1 Detection

The SPARC/CPU-8VT is configured by default for an automatic detection of VMEbus slot-1 position (SW8-1 is OFF).

IMPORTANT

Automatic VMEbus slot-1 detection will function properly only if all VMEbus boards installed in the system support this feature.

It is necessary that all boards installed in the system drive the VMEbus BG3OUT* signal at power-up to support the automatic VME slot-1 detection.
To disable this automatic VMEbus slot-1 detection feature, turn SW8-1 to ON.
If automatic detection of VMEbus slot-1 position is turned off (SW8-1 is ON), then SW8-2 is used to enable the VMEbus slot-1 controller functions of the SPARC/CPU-8VT.

IMPORTANT

Before installing the SPARC/CPU-8VT in a miniforce chassis, first disable the VMEbus system controller function by setting switch SW8-2 to ON. Ensure that SW8-1 is turned to ON to disable the automatic detection of VMEbus slot-1.

1.3.2 VMEbus SYSRESET

SYSRESET Input

A SYSRESET received from VMEbus generates an on-board RESET if switch SW7-2 is OFF (default setting). When SW7-2 is ON, the SYSRESET received from the VMEbus does not generate an on-board RESET.

SYSRESET Output

A SYSRESET signal is generated to the VMEbus when an on-board local SBus reset occurs on the SPARC/CPU-8VT (e.g. the front panel reset key is toggled or power failure is detected). This SYSRESET signal can be disabled by setting switch SW7-3 to ON.
As written in the VME specification, each board must assert SYSRESET output at power-up when the power supply reaches 3 V until power is stable. This feature is enabled by default (SW7-1 is OFF). It can be disabled by setting SW7-1 to ON.

1.3.3 Serial Ports

By default, both serial ports are configured as RS-232 interfaces. It is also possible to configure these ports as RS-422 interfaces. This optional configuration is achieved with the special FORCE Hybrid FH-003 or FH-422T.

The table 1 “Default Switch Settings” on page 3 shows the necessary switch settings for RS-232 operation, where SW4 controls serial port A and SW5 controls serial port B. Ensure that the switches are set accordingly.

1.3.4 RESET and ABORT Key Enable

By default, the RESET and ABORT key functions on the front panel are enabled. To disable the RESET or the ABORT key functions on the front panel, set switches SW6-4 (RESET) and SW7-4 (ABORT) to ON.

1.3.5 Boot Flash Memory Write Protection

Both boot flash memories are write-protected via the switch SW9-1. When SW9-1 is OFF, the devices are write-protected (default setting).

1.3.6 User Flash Memory Write Protection

The optional user flash memories are write-protected via SW9-2. When SW9-2 is OFF, the user flash EPROMs are write-protected (default setting).

1.3.7 Reserved Switches

SW4-4, SW5-4, SW8-3, and SW9-4 are reserved for test purposes. They must be OFF.

1.3.8 Floppy Interface or SCSI #2 Availability on P2

The availability of both the floppy and SCSI #2 devices at the same time depends on the availability of a 5-row P2 connector. When using a 3-row P2 connector (factory option), you have the choice of either the floppy or the SCSI #2 on P2. In the following it is described how to configure the board for floppy or SCSI #2:

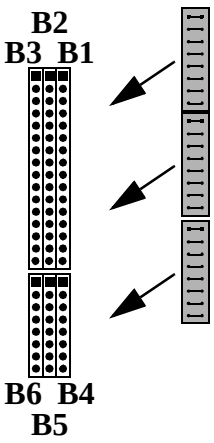
Via a 3-piece configuration switch matrix, it is possible for either the floppy interface or the SCSI #2 to be available on the VME P2 connector on row C:

- For the floppy interface on row C plug the switch matrix into sockets B3/B2 and B6/B5. This is the default setting.
- For the SCSI #2 interface on row C plug the switch matrix into sockets B2/B1 and B5/B4.

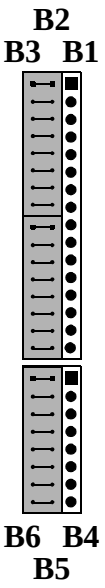
NOTICE

- If you use an IOBP-DS, the switch matrix must be located on B2/B1 and B5/B4 in order to route SCSI #2 to P2 row C.
- If you use an IOBP-10, the switch matrix must be located on B3/B2 and B6/B5 in order to route the floppy interface to P2 row C.

Figure 2 **Floppy or SCSI #2 Availability on P2**

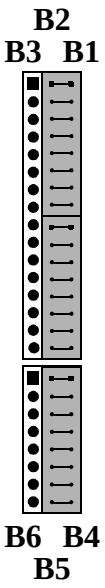


- Floppy interface on row C if the switch matrix is plugged in B3/B2 and B6/B5:



This configuration must be used when using an IOBP-10.

- SCSI #2 interface on row C if the switch matrix is plugged in B2/B1 and B5/B4:



This configuration must be used when using an IOBP-DS.

1.3.9 Network Interface Selection (NIS) for Ethernet

The Ethernet is selected either via the twisted pair connector or the AUI (Attachment Unit Interface).

- When you boot your system and a connection exists with an AUI network, then the AUI is automatically selected, i.e. when you have a successful connection with a network, the AUI is used.
- When you have no connection with the network, then the twisted pair is selected. This is valid for both Ethernet #1 and Ethernet #2. The Ethernet #1 channel and the Ethernet #2 channel function independently of each other. For both Ethernet interfaces there is one Ethernet address. This means that you are not allowed to connect both interfaces to one physical cable.

IMPORTANT

The Ethernet #2 AUI interface on P2 depends on the availability of a 5-row P2 connector. On the 3-row P2 connector (factory option), only Ethernet #1 AUI-port is available.

1.3.10 Parallel Port

The parallel port is only available on a 5-row P2 connector. When using a 3-row P2 connector (factory option), it is not available.

1.4 SCSI Configuration

In the following 2 sections the SCSI #1 termination or the SCSI #2 termination respectively are described.

1.4.1 SCSI #1 Termination

The SCSI #1 bus is accessible via the CPU board's front-panel SCSI #1 connector and via row A of the VMEbus P2 connector. Therefore, the CPU board holds 2 distinct SCSI bus terminations to enable correct termination of the SCSI #1 bus. Associated to the 2 terminations there are 2 switches – SW6-1 and SW6-2 – which allow easy selection of a valid SCSI #1 bus configuration.

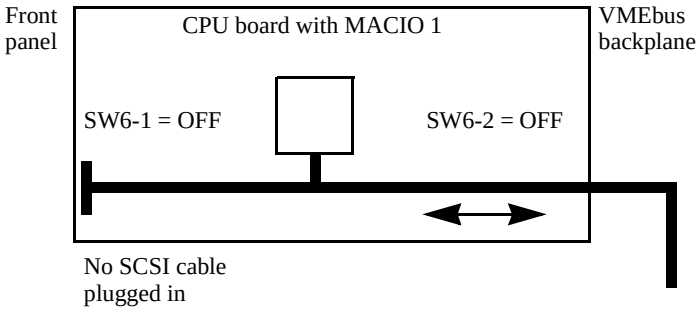
There are 3 valid CPU board switch settings corresponding to valid SCSI #1 bus configurations. The respective SCSI #1 bus configuration is determined by the cable connectors. There are the following 3 possibilities:

- cable connector to the VMEbus P2 connector,
- cable connector to the front panel,
- or a cable connector to the VMEbus P2 connector and the front panel.

Each of the following configuration descriptions starts with identifying the SCSI #1 bus configuration being covered and ends with defining the correct switch setting corresponding to the considered configuration.

Configuration 1

- The configuration 1 is covered by the default switch setting. The CPU board is located at an endpoint of the SCSI #1 bus, the SCSI #1 bus is extended via the VMEbus P2 connector, but no SCSI cable is plugged into the front-panel SCSI connector:



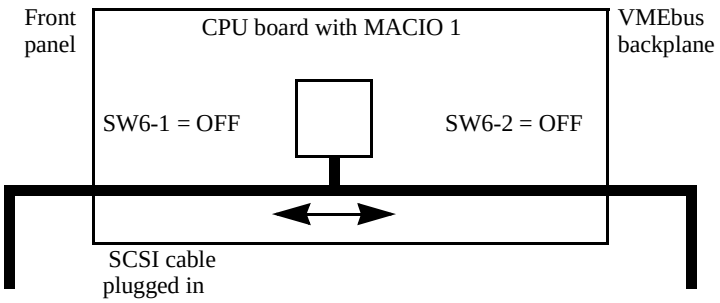
In this configuration:

– SW6-1 must be set to OFF = SCSI-Term front panel automatic (default “OFF”, see page 4)

– and SW6-2 must be set to OFF = disabled (default “OFF”, see page 4).

Configuration 2

- The configuration 2 is also covered by the default switch setting. The CPU board is not located at an endpoint of the SCSI #1 bus, the SCSI 1 bus is extended via the VMEbus P2 connector and via the front-panel SCSI connector:



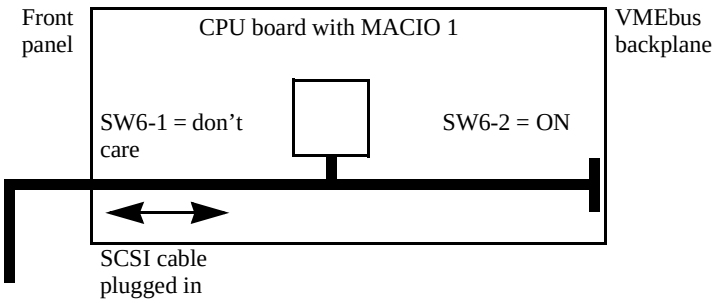
In this configuration:

– SW6-1 must be set to OFF = SCSI-Term front panel automatic (default “OFF”, see page 4)

– and SW6-2 must be set to OFF (default “OFF”, see page 4).

Configuration 3

• In configuration 3 the CPU board is located at an endpoint of the SCSI #1 bus and the VMEbus P2 connector is not used for SCSI #1 bus signalling, but the SCSI #1 bus is extended via the front-panel connector:



In this configuration

– both settings of SW6-1 are valid

– and SW6-2 must be set to ON = enabled (default “OFF”, see page 4).

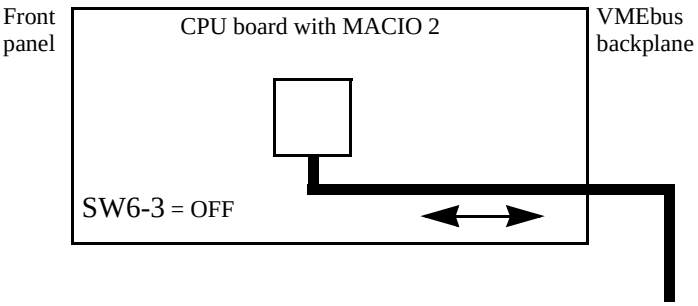
Since in this configuration the SCSI #1 bus is extended via the front-panel connector setting SW6-1 to ON = SCSI-Term front panel disabled, termination reflects this configuration explicitly.

1.4.2 SCSI #2 Termination

The SCSI #2 bus is only available on row C of the VMEbus P2 connector if it is enabled via switch matrix instead of floppy interface. It is terminated – i.e. it is at one endpoint of the SCSI #2 bus – if SW6-3 is set appropriately: OFF = enabled termination (default “OFF”, see page 4).

Configuration 1

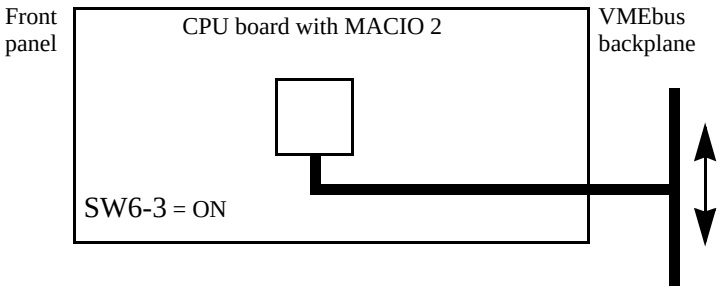
- The configuration 1 is covered by the default switch setting: The board is located at an endpoint of the SCSI #2 bus, i.e., the SCSI #2 bus is extended via the VMEbus P2 connector:



In this configuration SW6-3 must be set to OFF = enabled termination (default “OFF”, see page 4).

Configuration 2

- In configuration 2 the CPU board is not located at an endpoint of the SCSI #2 bus, i.e., the SCSI #2 bus is accessed via the VMEbus P2 connector:



In this configuration SW6-3 must be set to ON = disabled termination (default “OFF”, see page 4).

1.5 Connectors

The SPARC/CPU-8VT connectors are listed in the following table.

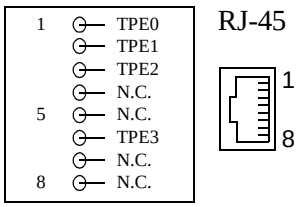
Table 2 SPARC/CPU-8VT Connectors

Function	Location	Type	Manufacturer part number
Ethernet #1 (twisted pair)	Front panel	RJ-45	AMP 555131-1
Ethernet #2 (twisted pair)	Front panel	RJ-45	AMP 555131-1
Serial ports A + B	Front panel	26-pin micro D-Sub	AMP 749831-2
SCSI #1	Front panel	50-pin micro D-Sub	AMP 749831-5
Keyboard/mouse	Front panel	8-pin mini DIN	AMP 749232-1
SBus slot2 (SBus slave select 1)	P3	96-pin SMD	FUJITSU FCN-234J096-G/V
SBus slot3 (SBus slave select 2)	P4	96-pin SMD	FUJITSU FCN-234J096-G/V
VMEbus P1	P1	96-pin VGA	Various
VMEbus P2	P2	96-pin VGA	Various

1.5.1 Twisted Pair Ethernet Connector Pinout

The following figure shows the pinout of the twisted pair Ethernet connector. The pinout for both of the connectors is identical.

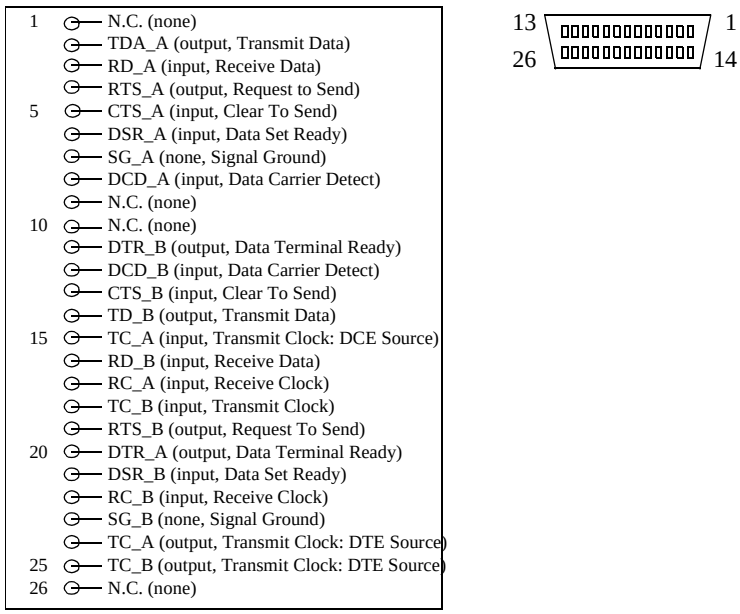
Figure 3 Twisted Pair Ethernet Connector Pinout



1.5.2 Serial Port A and B Connector Pinout

The following figure shows the pinout of the serial port connector.

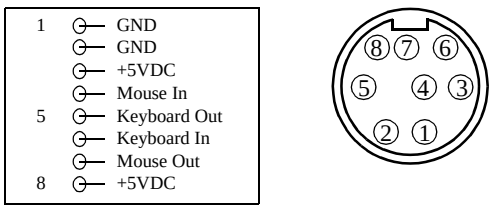
Figure 4 Serial Port A and B Connector Pinout


1 N.C. (none)
TDA_A (output, Transmit Data)
RD_A (input, Receive Data)
RTS_A (output, Request to Send)
5 CTS_A (input, Clear To Send)
DSR_A (input, Data Set Ready)
SG_A (none, Signal Ground)
DCD_A (input, Data Carrier Detect)
N.C. (none)
10 N.C. (none)
DTR_B (output, Data Terminal Ready)
DCD_B (input, Data Carrier Detect)
CTS_B (input, Clear To Send)
TD_B (output, Transmit Data)
15 TC_A (input, Transmit Clock: DCE Source)
RD_B (input, Receive Data)
RC_A (input, Receive Clock)
TC_B (input, Transmit Clock)
RTS_B (output, Request To Send)
20 DTR_A (output, Data Terminal Ready)
DSR_B (input, Data Set Ready)
RC_B (input, Receive Clock)
SG_B (none, Signal Ground)
TC_A (output, Transmit Clock: DTE Source)
25 TC_B (output, Transmit Clock: DTE Source)
26 N.C. (none)
13
1
26
14

1.5.3 Keyboard/Mouse Connector Pinout

The keyboard and mouse port is available on the front panel via a mini DIN connector.

Figure 5 Keyboard/Mouse Connector Pinout



1.5.4 VME P2 Connector Pinout

The SCSI #2 interface is an alternative to the FDC interface on row C. The signals for rows Z and D are not available on the 3-row P2 connector (factory option).

Figure 6 VME P2 Connector Pinout

Z	A		C	D
CENTR DS	SCSI#1-D0	1	FDC HD IN/OUT (SCSI#2-D0*)	NC
GND	SCSI#1-D1		FDC HEAD LOAD (SCSI#2-D1*)	NC
CENTR D0	SCSI#1-D2		FDC NC (SCSI#2-D2*)	SCSI#2-D0
GND	SCSI#1-D3		FDC INDEX (SCSI#2-D3*)	SCSI#2-D1
CENTR D1	SCSI#1-D4	5	FDC DS0 (SCSI#2-D4*)	SCSI#2-D2
GND	SCSI#1-D5		NC (SCSI#2-D5*)	SCSI#2-D3
CENTR D2	SCSI#1-D6		NC (SCSI#2-D6*)	SCSI#2-D4
GND	SCSI#1-D7		FDC MOTORON (SCSI#2-D7*)	SCSI#2-D5
CENTR D3	SCSI#1-DP		FDC DIR (SCSI#2-DP*)	SCSI#2-D6
GND	GND	10	FDC STEP (SCSI#2-ATTN*)	SCSI#2-D7
CENTR D4	GND		FDC WDATA (SCSI#2-BSY*)	SCSI#2-DP
GND	GND		FDC WGATE (SCSI#2-ACK*)	TERMPWR#2
CENTR D5	TERMPWR#1		FDC TRACK00 (SCSI#2-RST*)	SCSI#2-ATTN
GND	GND		FDC WPROT (SCSI#2-MSG*)	SCSI#2-BSY
CENTR D6	GND	15	FDC RDATA (SCSI#2-SEL*)	SCSI#2-ACK
GND	SCSI#1-ATTN		FDC SIDESEL (SCSI#2-CD*)	SCSI#2-RST
CENTR D7	GND		FDC DISKCH/RDY (SCSI#2-REQ*)	SCSI#2-MSG
GND	SCSI#1-BSY		FDC EJECT (SCSI#1-IO*)	SCSI#2-SEL
CENTR ACK	SCSI#1-ACK		ETH#1_POW	SCSI#2-CD
GND	SCSI#1-RST	20	GND (TERMPWR#2*)	SCSI#2-REQ
CENTR BSY	SCSI#1-MSG		GND	SCSI#1-IO
GND	SCSI#1-SEL		ETH#1_REC+	CENTR_SLCTIN
CENTR PE	SCSI#1-CD		ETH#1_REC-	MOUSEOUT
GND	SCSI#1-REQ		ETH#1_TRA+	ETH#2_POW
CENTR AF	SCSI#1-IO	25	ETH#1_TRA-	ETH#2_REC+
GND	MOUSEIN		ETH#1_COL+	ETH#2_REC-
CENTR INIT	TXD_KBD		ETH#1_COL-	ETH#1_TRA+
GND	RXD_KBD		GND	ETH#1_TRA-
CENTR ERR	TXD_A		TXD_B	ETH#1_COL+
GND	RXD_A	30	RXD_B	ETH#1_COL-
CENTR SLCT	RTS_A		RTS_B	NC
GND	CTS_A	32	CTS_B	NC

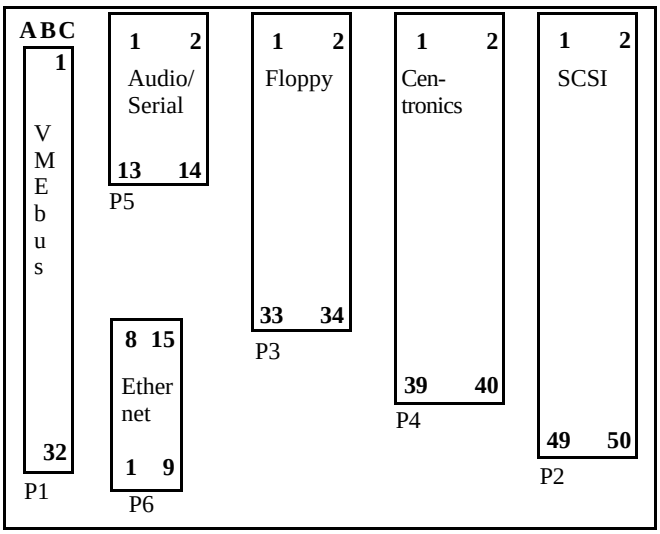
* The SCSI #2 interface is an alternative to the FDC interface (see section 1.3.8 “Floppy Interface or SCSI #2 Availability on P2” on page 8).

1.6 IOBP-10

IOBP-10 and IOBP-DS can be plugged to the back side of a VMEbus backplane. They only fit into 3-row backplanes. Any attempt to attach them to a 5-row backplane connector might damage the backplane.

The IOBP-10 is an I/O back panel on VMEbus P2 with flat cable connectors for SCSI, serial I/O, Centronics/floppy interface, and a micro D-Sub connector for the Ethernet #1 interface. The Centronics interface on the IOBP-10 is not supported by the SPARC/CPU-8VT. This back panel can be plugged into the VMEbus P2 connector. The diagram below shows all connectors. The IOBP-10 back panel and the IOBP-DS are especially designed for the SPARC/CPU-8VT. Do not use any other I/O back panels on the SPARC/CPU-8VT.

Figure 7 The IOBP-10 Back Panel



1.6.1 Jumper Setting for IOBP-10

NOTICE

- Ensure that the configuration switch matrix is plugged into sockets B3/B2 and B6/B5, that is the configuration for floppy interface on P2 (see section 1.3.8 “Floppy Interface or SCSI #2 Availability on P2” on page 8).
- The IOBP-10 back panel and the IOBP-DS are especially designed for the SPARC/CPU-8VT. Do not use any other I/O back panels on the SPARC/CPU-8VT.

1.6.2 IOBP-10 Connector Pinouts

Figure 8 IOBP-10 P1 Pinout

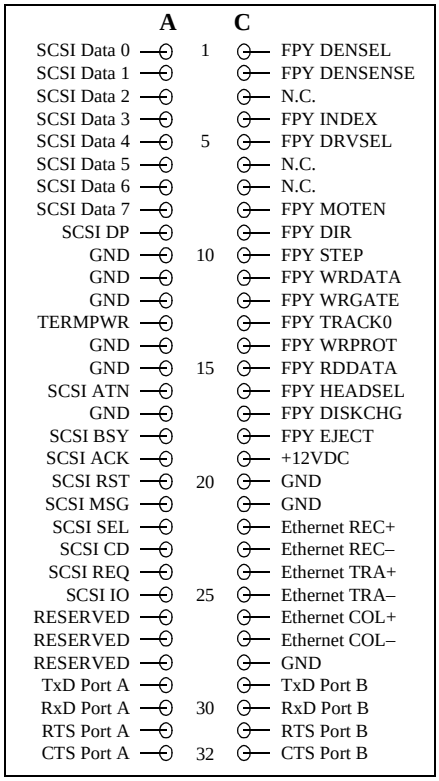


Figure 9 IOBP-10 P2 Pinout (SCSI #1)

GND	1	2	SCSI #1 Data 0
GND	3	4	SCSI #1 Data 1
GND	5	6	SCSI #1 Data 2
GND	7	8	SCSI #1 Data 3
GND	9	10	SCSI #1 Data 4
GND	11	12	SCSI #1 Data 5
GND	13	14	SCSI #1 Data 6
GND	15	16	SCSI #1 Data 7
GND	17	18	SCSI #1 DP
GND	19	20	GND
GND	21	22	GND
GND	23	24	GND
N.C.	25	26	TERMPWR #1
GND	27	28	GND
GND	29	30	GND
GND	31	32	SCSI #1 ATN
GND	33	34	GND
GND	35	36	SCSI #1 BSY
GND	37	38	SCSI #1 ACK
GND	39	40	SCSI #1 RST
GND	41	42	SCSI #1 MSG
GND	43	44	SCSI #1 SEL
GND	45	46	SCSI #1 CD
GND	47	48	SCSI #1 REQ
GND	49	50	SCSI #1 IO

Figure 10 **IOBP-10 P3 Pinout (Floppy)**

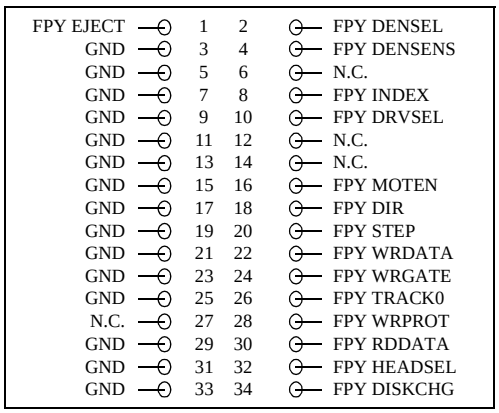

FPY EJECT 1 2 FPY DENSEL
GND 3 4 FPY DENSENS
GND 5 6 N.C.
GND 7 8 FPY INDEX
GND 9 10 FPY DRVSEL
GND 11 12 N.C.
GND 13 14 N.C.
GND 15 16 FPY MOTEN
GND 17 18 FPY DIR
GND 19 20 FPY STEP
GND 21 22 FPY WRDATA
GND 23 24 FPY WRGATE
GND 25 26 FPY TRACK0
N.C. 27 28 FPY WRPROT
GND 29 30 FPY RDDATA
GND 31 32 FPY HEADSEL
GND 33 34 FPY DISKCHG

Figure 11 **IOBP-10 P5 Pinout (Serial A and B)**

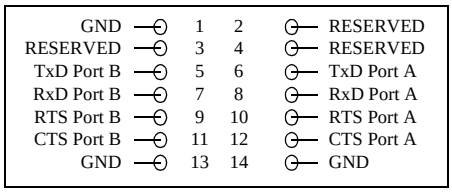
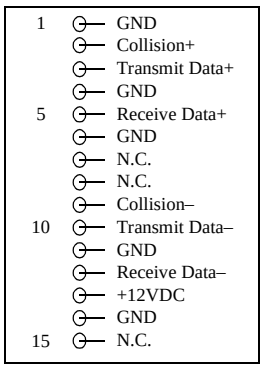

GND 1 2 RESERVED
RESERVED 3 4 RESERVED
TxD Port B 5 6 TxD Port A
RxD Port B 7 8 RxD Port A
RTS Port B 9 10 RTS Port A
CTS Port B 11 12 CTS Port A
GND 13 14 GND

Figure 12 **IOBP-10 P6 Pinout (Ethernet #1 – AUI)**

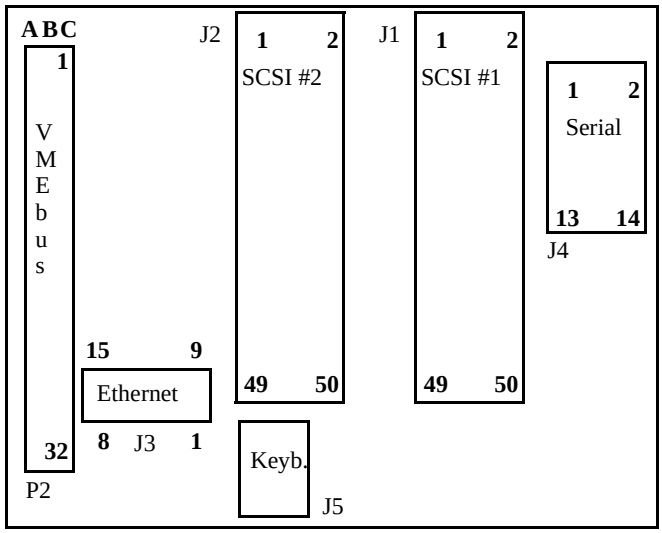


1.7 IOBP-DS

IOBP-10 and IOBP-DS can be plugged to the back side of a VMEbus backplane. They only fit into 3-row backplanes. Any attempt to attach them to a 5-row backplane connector might damage the backplane.

The IOBP-DS is an I/O back panel on VMEbus P2 with flat cable connectors for SCSI #1, SCSI #2, serial I/O, keyboard/mouse, and a micro D-Sub connector for the Ethernet #1 interface (AUI). This back panel can be plugged into the VMEbus P2 connector. The diagram below shows all connectors. The IOBP-I/O back panel and the IOBP-DS are especially designed for the SPARC/CPU-8VT. Do not use any other I/O back panels on the SPARC/CPU-8VT.

Figure 13 The IOBP-DS Back Panel



1.7.1 Jumper Setting for IOBP-DS

NOTICE

- Please ensure that the configuration switch matrix is plugged into sockets B2/B1 and B5/B4, that is the configuration for dual SCSI interface on P2 (5-row connector) (see section 1.3.8 “Floppy Interface or SCSI #2 Availability on P2” on page 8).
- The IOBP-DS back panel and the IOBP-10 are especially designed for the SPARC/CPU-8VT. Do not use any other I/O back panels on the SPARC/CPU-8VT.

1.7.2 IOBP-DS Connector Pinouts

Figure 14 IOBP-DS P2 Pinout

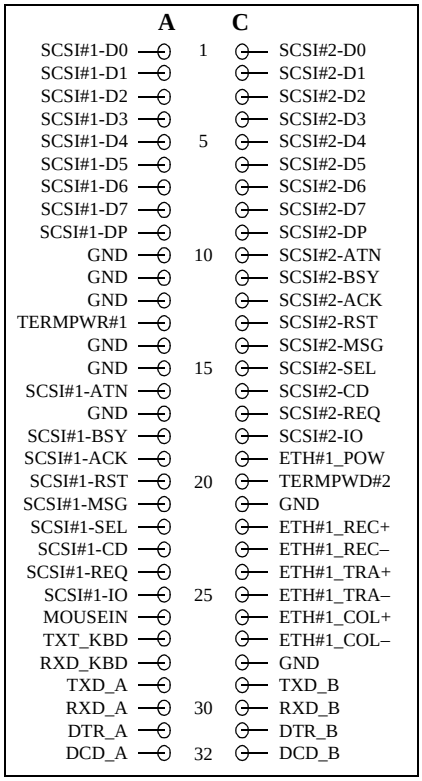


Figure 15 IOBP-DS J1 Pinout (SCSI #1)

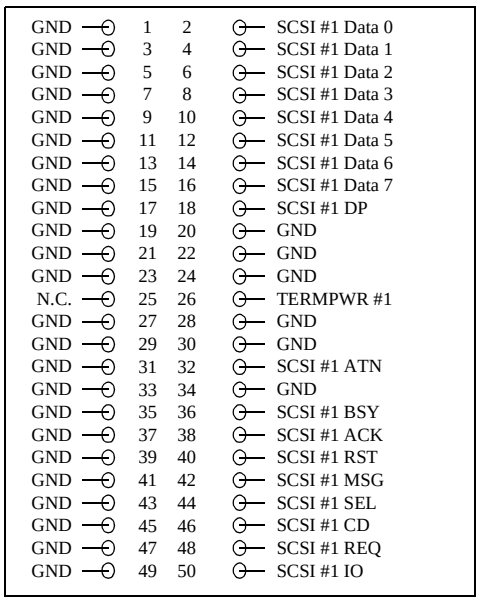

GND 1 2 SCSI #1 Data 0
GND 3 4 SCSI #1 Data 1
GND 5 6 SCSI #1 Data 2
GND 7 8 SCSI #1 Data 3
GND 9 10 SCSI #1 Data 4
GND 11 12 SCSI #1 Data 5
GND 13 14 SCSI #1 Data 6
GND 15 16 SCSI #1 Data 7
GND 17 18 SCSI #1 DP
GND 19 20 GND
GND 21 22 GND
GND 23 24 GND
N.C. 25 26 TERMPWR #1
GND 27 28 GND
GND 29 30 GND
GND 31 32 SCSI #1 ATN
GND 33 34 GND
GND 35 36 SCSI #1 BSY
GND 37 38 SCSI #1 ACK
GND 39 40 SCSI #1 RST
GND 41 42 SCSI #1 MSG
GND 43 44 SCSI #1 SEL
GND 45 46 SCSI #1 CD
GND 47 48 SCSI #1 REQ
GND 49 50 SCSI #1 IO

Figure 16 IOBP-DS J2 Pinout (SCSI #2)

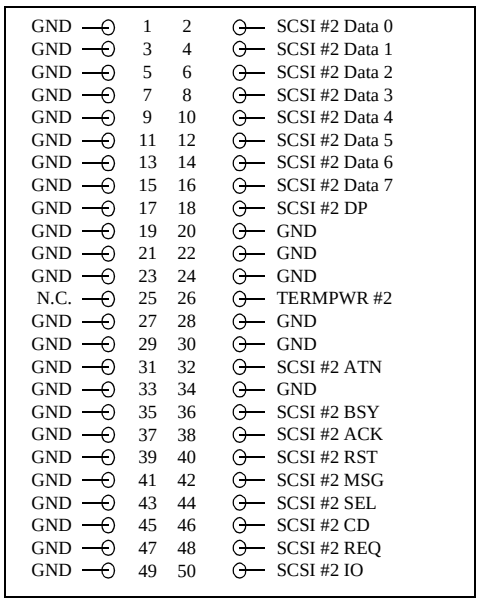

GND 1 2 SCSI #2 Data 0
GND 3 4 SCSI #2 Data 1
GND 5 6 SCSI #2 Data 2
GND 7 8 SCSI #2 Data 3
GND 9 10 SCSI #2 Data 4
GND 11 12 SCSI #2 Data 5
GND 13 14 SCSI #2 Data 6
GND 15 16 SCSI #2 Data 7
GND 17 18 SCSI #2 DP
GND 19 20 GND
GND 21 22 GND
GND 23 24 GND
N.C. 25 26 TERMPWR #2
GND 27 28 GND
GND 29 30 GND
GND 31 32 SCSI #2 ATN
GND 33 34 GND
GND 35 36 SCSI #2 BSY
GND 37 38 SCSI #2 ACK
GND 39 40 SCSI #2 RST
GND 41 42 SCSI #2 MSG
GND 43 44 SCSI #2 SEL
GND 45 46 SCSI #2 CD
GND 47 48 SCSI #2 REQ
GND 49 50 SCSI #2 IO

Figure 17 IOBP-DS J3 Pinout (Ethernet #1 – AUI)

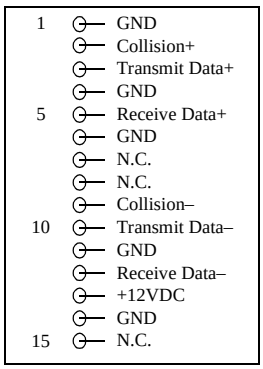


Figure 18 IOBP-DS J4 Pinout (Serial A and B)

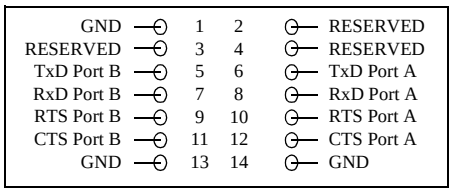
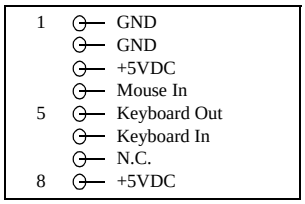

GND 1 2 RESERVED
RESERVED 3 4 RESERVED
TxD Port B 5 6 TxD Port A
RxD Port B 7 8 RxD Port A
RTS Port B 9 10 RTS Port A
CTS Port B 11 12 CTS Port A
GND 13 14 GND

Figure 19 IOBP-DS J5 Pinout (Keyboard/mouse)



1.8 Ethernet Address and Host ID

In order to see the Ethernet address and host ID, type the following command at the prompt:

```
ok banner
```

The information below explains how the SPARC/CPU-8VT Ethernet address and the host ID are determined.

Figure 20 **The 48-bit (6-byte) Ethernet Address**

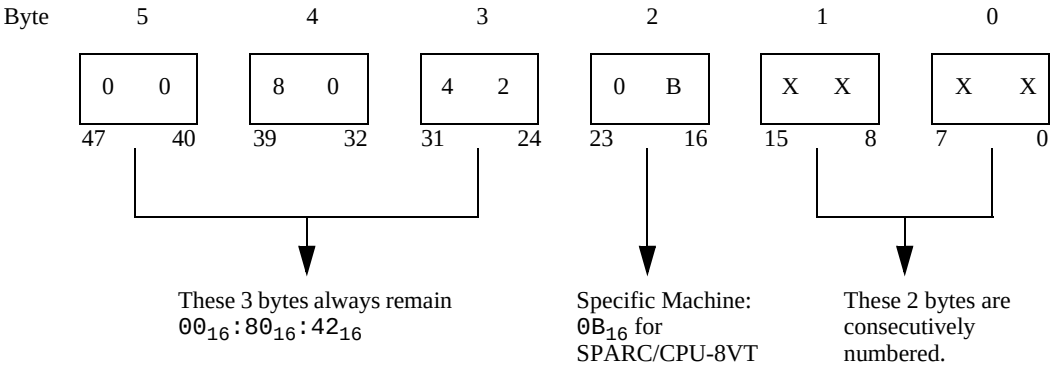
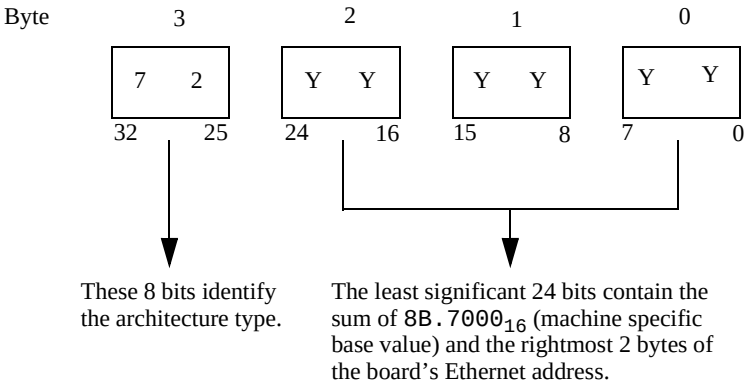


Figure 21 **The 32-bit (4-byte) Host ID**


Byte 3 2 1 0
7 2
Y Y
Y Y
Y Y
32 25
24 16
15 8
7 0
These 8 bits identify the architecture type.
The least significant 24 bits contain the sum of 8B.7000₁₆ (machine specific base value) and the rightmost 2 bytes of the board's Ethernet address.

1.9 OpenBoot Firmware

The following tasks are described in this section:

- Boot the system
- Run diagnostics
- Display system information
- Reset the system
- OpenBoot help

For detailed information concerning OpenBoot, see the *OPEN BOOT PROM 2.0 MANUAL SET*.

1.9.1 Boot the System

The most important function of OpenBoot firmware is the booting of the system. Booting is the process of loading and executing a stand-alone program such as the operating system. After it is powered on, the system usually boots automatically after it has passed the power-on self test (POST). This occurs without user intervention.
If necessary, you can explicitly initiate the boot process from the Open-Boot command interpreter. Automatic booting uses the default boot device specified in nonvolatile RAM (NVRAM); user initiated booting uses either the default boot device or one specified by the user.

To boot the system from the default boot device, enter the following command at the Forth monitor prompt `ok`:

```
ok boot
```

If you are at the restricted monitor prompt `>`, enter:

```
> b
```

The boot command has the following format:
`boot [device-specifier] [filename] [-ah]`

Optional Boot Parameters

IMPORTANT

These options are specific to the operating system and may differ from system to system.

`[device-specifier]`
The name (full path or alias) of the boot device. Typical values are `cdrom`, `disk`, `floppy`, `net`, or `tape`.

[*filename*]
The name of the program to be booted. *`filename`* is relative to the root of the selected device. If no filename is specified, the boot command uses the value of *`boot-file`* NVRAM parameter. The NVRAM parameters used for booting are described in the following section.

`[-a]`
`-a` prompt interactively for the device and name of the boot file.

`[-h]`
`-h` halt after loading the program.

Devices to boot from

To explicitly boot from the internal disk using the Forth monitor enter:

```
ok boot disk
```

At the restricted monitor prompt enter:

```
> b disk
```

To retrieve a list of all device alias definitions, type `devalias` at the Forth monitor command prompt. The following table lists some typical device aliases:

Table 3 **Device Alias Definitions**

Alias	Description
`disk`	Default disk (1st internal) SCSI-ID 3
`disk3`	First internal disk SCSI-ID 3
`disk2`	Additional internal disk SCSI-ID 2
`disk1`	External disk SCSI-ID 1
`disk0`	External disk SCSI-ID 0
`tape`	First tape drive SCSI-ID 4
`tape0`	First tape drive SCSI-ID 4
`tape1`	Second tape drive SCSI-ID 5

Table 3 **Device Alias Definitions (cont.)**

Alias	Description
`cdrom`	CD-ROM partition d, SCSI-ID 6
`net`	Ethernet
`floppy`	Floppy drive

1.9.2 NVRAM Boot Parameters

The OpenBoot firmware holds configuration parameters in NVRAM. At the Forth monitor prompt, type `printenv` to see a list of all available configuration parameters. The OpenBoot command `setenv` may be used to set these parameters:
`setenv` *`[configuration parameter] [value]`*

This information refers only to those configuration parameters which are involved in the boot process. The following table lists these parameters.

Table 4 **Setting Configuration Parameters**

Parameter	Default value	Description
`auto-boot?`	`true`	If `true`, automatic booting after power-on or reset
`boot-device`	`disk`	Device from which to boot
`boot-file`	`empty string`	File to boot
`diag-switch?`	`false`	If `true`, run in diagnostic mode
`diag-device`	`net`	Device from which to boot in diagnostic mode
`diag-file`	`empty string`	File to boot in diagnostic mode

When booting an operating system or another stand-alone program, and neither a boot device nor a filename is supplied, the `boot` command of the Forth monitor takes the omitted values from the NVRAM configuration parameters. If the parameter `diag-switch?` is `false`, `boot-device`, and `boot-file` are used. Otherwise, the OpenBoot firmware uses `diag-device` and `diag-file` for booting.
For detailed information on all NVRAM configuration parameters, see the *OPEN BOOT PROM 2.0 MANUAL SET.*

1.9.3 Diagnostics

At power-on or after reset the OpenBoot firmware executes POST. If the NVRAM configuration parameter `diag-switch?` is `true` for each test, a message is displayed on a terminal connected to the serial I/O port A. If the system does not work correctly, error messages are displayed indicating the problem. After POST the OpenBoot firmware boots an operating system or enters the Forth monitor, if the NVRAM configuration parameter `auto-boot?` is `false`.
The Forth monitor includes several diagnostic routines. These on-board tests let you check devices such as network controller, SCSI devices, floppy disk system, memory, clock, and installed SBus cards. User installed devices can be tested if their firmware includes a self-test routine. The table below lists several diagnostic routines.

Table 5 Diagnostic Routines

Command	Description
`probe-scsi`	Identify devices connected to the on-board SCSI bus
`probe-scsi-all` *`[device-path]`*	Perform probe-scsi on all SCSI buses installed in the system below the specified device tree node. (If *device-path* is omitted, the root node is used).
`test` *`device-specifier`*	Execute the specified device's self-test method. *`device-specifier`* may be a device path name or a device alias. For example: `test` *`net`* - test network connection `test` *`/memory`* - test number of MByte specified in the self-test-#megs NVRAM parameter or test all of memory if `diag-switch?` is `true`
`test-all` *`[device-specifier]`*	Test all devices (that have a built-in self-test method) below the specified device tree node. (If *device-path* is omitted, the root node is used.)
`watch-`*`clock`*	Monitor the clock function
`watch-`*`net`*	Monitor network connection

Examples:

SCSI bus To check the on-board SCSI bus for connected devices, enter:

```
ok probe-scsi
Target 0
Unit 0 Disk SEAGATE ST31230W 0456
ok
```

All SCSI busses

To test all the SCSI busses installed in the system, enter the following (The actual response depends on the devices on the SCSI busses):

```
ok probe-scsi-all
/iommu@0,10000000/sbus@0,10001000/esp@2,100000

Target 0
Unit 0 Disk SEAGATE ST31230W 0456

/iommu@0,10000000/sbus@0,10001000/espdma@4,8400000/esp@4,8800000

Target 5
Unit 0 Removable Read Only device TOSHIBA CD-ROM XM-4101TA1084
ok
```

Single device

To test a single installed device enter:

```
ok test device-specifier
```

This executes the `self-test` device method of the specified device node.
`device-specifier` may be a device path name or a device alias as described in Table 3, “Device Alias Definitions,” on page 24. The response depends on the self-test of the device node.

Group of Devices

To test a group of installed devices enter:

```
ok test-all
```

All devices below the root node of the device tree are tested. The response depends on the devices having a self-test routine. If a device specifier option is supplied at the command line, all devices below the specified device tree node are tested.

Memory

When using the memory testing routine, the system tests the number of MByte of memory specified in the NVRAM configuration parameter `self-test-#megs`. If the NVRAM configuration parameter `diag-switch?` is `true`, the whole memory is tested.

```
ok test /memory
testing 32 megs of memory at addr 0 27
ok
```

The command `test-memory` is equivalent to `test /memory`. In the above-mentioned example, the first number (`0`) is the base address of the memory bank to be tested, the second number (`27`) is the number of the remaining MByte.

- If the CPU board works correctly, the memory is erased and tested and the **ok** prompt will appear.
- If the PROM or the on-board memory does not work, one of several potential error messages indicating the problem will appear.

Clock

To test the clock function enter:

```
ok watch-clock
Watching the ‘seconds’ register of the real time clock
chip.
It should be ‘ticking’ once a second.
Type any key to stop.
22
ok
```

The system responds by incrementing a number once a second. Press any key to stop the test.

Network

To monitor the network connection enter:

```
ok watch-net
Using AUI Ethernet Interface
Lance register test -- succeeded.
Internal loopback test -- succeeded.
External loopback test -- succeeded.
Looking for Ethernet packets.
‘.’ is a good packet. ‘X’ is a bad packet.
Type any key to stop.
...........X.........................X.............
ok
```

The system monitors the network traffic displaying

- a dot (.) when receiving a valid packet
- and an X when receiving a packet with an error which can be detected by the network hardware interface.

1.9.4 Display System Information

The Forth monitor provides several commands to display system information. These commands let you display the system banner, the Ethernet address for the Ethernet controller, the contents of the ID PROM, and the version number of the OpenBoot firmware.
The ID PROM contains specific information to the individual machine, including the serial number, date of manufacture, and assigned Ethernet address.

The following table lists these commands:

Table 6 **Commands to display System Information**

Command	Description
`banner`	Displays system banner
`show-sbus`	Displays list of installed and probed SBus devices
`.enet-addr`	Displays current Ethernet address
`.idprom`	Displays ID PROM contents, formatted
`.traps`	Displays a list of SPARC trap types
`.version`	Displays version and date of the boot PROM
`show-devs`	Displays a list of all device tree nodes
`devalias`	Displays a list of all device aliases

1.9.5 Reset the System

If your system needs to be reset

- press the reset button on the front panel
- or, if you are in the Forth monitor, type **reset** on the command line.

```
ok reset
```

The system immediately begins executing the power-on self test (POST) and the initialization procedures. When the POST is completed, the system either boots automatically or enters the Forth monitor, just as it would have done after a power-on cycle.

1.9.6 OpenBoot Help

The Forth monitor contains an on-line help which can be activated by entering `help`:

```
ok help
Enter ‘help command-name’ or ‘help category-name’ for more help
(Use ONLY the first word of a category description)
Examples: help select -or- help line
Main categories are:
File download and boot
Resume execution
Diag (diagnostic routines)
Power on reset
>-prompt
Floppy eject
Select I/O devices
Ethernet
System and boot configuration parameters
Line editor
Tools (memory,numbers,new commands,loops)
Assembly debugging (breakpoints,registers,disassembly,symbolic)
Sync (synchronize disk data)
Nvramrc (making new commands permanent)
ok
```

A list of all available help categories is displayed. These categories may also contain subcategories. To get help for special Forth words or subcategories just type `help [name]`.
The on-line help shows you the Forth word, the parameter stack before and after execution of the Forth word (before -- after), and a short description.
The on-line help of the Forth monitor is located in the boot PROM, that means that the on-line help does not exist for all Forth words.

Example:

How to get help for special Forth words or subcategories:

```
ok help tools
 Category: Tools (memory,numbers,new commands,loops)
 Subcategories are:
Memory access
Arithmetic
Radix (number base conversions)
Numeric output
Defining new commands
Repeated loops
ok
```

```
ok help memory
 Category: Memory access
dump ( addr length -- ) display memory at addr for length bytes
fill ( addr length byte -- ) fill memory starting at addr with byte
move ( src dest length -- ) copy length bytes from src to dest address
map? ( vaddr -- ) show memory map information for the virtual address
l? ( addr -- ) display the 32-bit number from location addr
w? ( addr -- ) display the 16-bit number from location addr
c? ( addr -- ) display the 8-bit number from location addr
l@ ( addr -- n ) place on the stack the 32-bit data at location addr
w@ ( addr -- n ) place on the stack the 16-bit data at location addr
c@ ( addr -- n ) place on the stack the 8-bit data at location addr
l! ( n addr -- ) store the 32-bit value n at location addr
w! ( n addr -- ) store the 16-bit value n at location addr
c! ( n addr -- ) store the 8-bit value n at location addr
ok
```

Product Error Report

PRODUCT:	SERIAL NO.:
DATE OF PURCHASE:	ORIGINATOR:
COMPANY:	POINT OF CONTACT:
TEL.:	EXT.:
ADDRESS: _____ _____ _____	
PRESENT DATE:	
AFFECTED PRODUCT: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS	AFFECTED DOCUMENTATION: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS
ERROR DESCRIPTION: _____ _____ _____ _____ _____ _____ _____ _____ _____ _____	

THIS AREA TO BE COMPLETED BY FORCE COMPUTERS:

DATE:

PR#:

RESPONSIBLE DEPT.: ❑ MARKETING ❑ PRODUCTION
ENGINEERING ➠ ❑ BOARD ❑ SYSTEMS

✉ Send this report to the nearest Force Computers headquarter listed on the address page.